EXHIBIT B

Exhibit B

Tutorial Background

1. Electric current flows in response to a voltage differential. In many cases the current is proportional to voltage, so the ratio of voltage divided by current is called resistance, expressed in ohms. Resistivity is the material property that measures the ability of a material to resist current flow, expressed in ohm centimeters. The reciprocal of resistivity is conductivity. Materials with high resistivity are said to be resistive; materials with high conductivity are said to be conductive. Good conductors, like metals, which allow current flow with generally negligible resistance, have very low resistivity. Insulators, which generally allow only negligible current flow, have very high resistivity. Some materials with resistivity intermediate between metals and insulators are called semiconductors ("semi" is Latin for "half").

2. Silicon is an example of a semiconductor, of interest in this case. Aluminum is an example of a metal of interest in this case. Silicon dioxide (called "oxide" for short) is an example of an insulator of interest in this case.

3. Semiconductors are either N type or P type depending upon the "doping". Dopants such as phosphorus are added to silicon to make it N type, because each phosphorus atom provides a free negative electron. Dopants such as boron are added to silicon to make it P type because each boron atom captures an electron, thereby providing a free positive hole, or missing electron. The concentration of such free carriers is equal to the concentration of dopants, so conductivity of silicon is proportional to dopant concentration. Resistivity is inversely proportional to dopant concentration.

4. Semiconductors can be doped when the material is melted to make a crystal, after which the crystal is sliced into "wafers" for the fabrication of electronic devices. During device fabrication, "local doping" is used to introduce additional dopant to selected regions of a semiconductor. Local doping uses ph0000otolithography, a process similar to photography, to print masking materials, which block the dopant except in the regions desired. Two methods of local doping are diffusion and implantation. Diffusion uses high temperatures to jiggle the dopant atoms and thereby penetrate into a semiconductor. Implantation accelerates dopant atoms to high energy for penetration into a semiconductor, like bullets.

5. For multiple doping processes, the similar type dopant concentrations add. P type and N type dopants cancel each other, so the net effective doping equals the lower concentration (N or P) subtracted from the higher concentration.

6. When silicon is carefully added (high temperature, very slowly) to a wafer, the additional silicon follows the same crystal structure as the wafer. This is called epitaxial silicon, or "epi" for short. Epi is lightly doped during growth for the devices of interest to this case.

7. When silicon is added quickly to a wafer, many small crystals form. This is called polycrystalline silicon, or "poly" for short ("poly" is Greek for "many"). Very heavily doped poly can be considered a metal.

8. A transistor is a device that has variable resistance. A transistor usually has 3 wires, or 3 metal connections. The resistance between two wires depends upon the current or voltage applied to the third wire (therefore "trans-resistance"). A transistor with the structure Metal - Oxide - Semiconductor is called an MOS transistor. These days the "M" is usually not metal but very heavily doped poly. The poly (and the electrical connection to the poly) is called the gate. The other two connections are called the source and the drain. The resistance between the source and the drain can be varied by varying the voltage on the gate. The "gate" opens and closes like a gate in response to voltage.

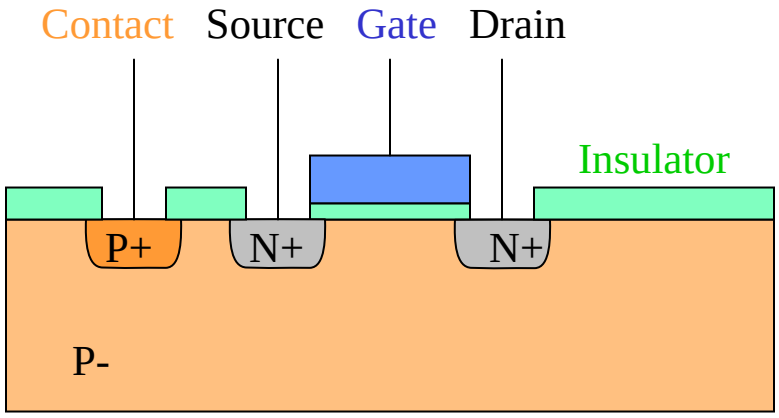
9. Transistors of interest to this case are used as a switch to turn a current on and off. With a large enough voltage (significantly greater than the "threshold" voltage) applied to the gate, the transistor is on, and the resistance between the source and drain is low. With a voltage less than the threshold voltage applied to the gate, the transistor is off, and negligible current flows. For the transistors in this case, a relatively larger voltage is applied to the drain. If the drain voltage is large enough, the transistor may fail, allowing current to flow even with the gate off. This "voltage breakdown" may destroy the transistor. Transistors can be designed to withstand relatively higher voltages without breakdown.

10. This case concerns the design structure of transistors that have relatively low resistance when on, and that are able to withstand relatively high drain voltage.

11. Claim 1 of the '075 patent is for an MOS transistor. MOS transistors are P type (PMOS) or N type (NMOS). An MOS transistor has a source and a drain separated by a gate. A PMOS transistor is constructed on an N type substrate with P type source and drain. An NMOS transistor is constructed on an P type substrate with N type source and drain.

12. Fig. 1 is a cross section sketch of the structure of an NMOS transistor.

Fig. 1



13. Because the source and drain are within the substrate, source and drain doping must necessarily be greater than substrate doping. Substrate doping in practice is typically much lower concentration than the source - drain, respectively indicated by minus and plus. Electrical contacts by metal are sketched as lines in Fig. 1, and will be omitted in the sequel. Labels will also be omitted in the sequel, with drain always to the right.

14. Electrical contact to silicon is facilitated by high doping. A heavily doped “contact” region for electrical connection to the substrate is sketched in Fig. 1.

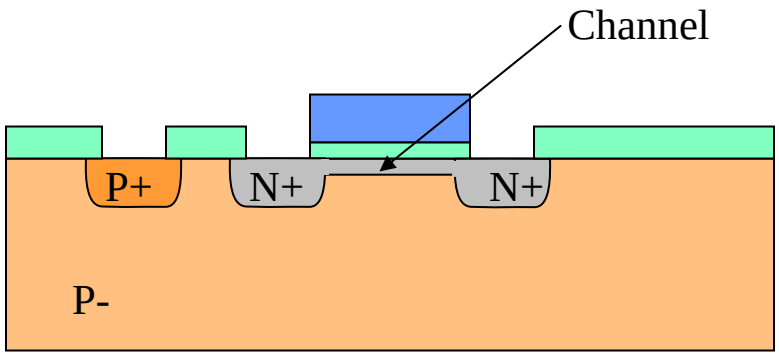
15. The oxide insulator material provides surface isolation.

16. MOS transistors are self isolated because the PN junctions are reverse-biased. PN junctions function as rectifiers, allowing current to flow only when forward-biased, when the P side has a voltage more positive than (or less negative than) the voltage on the N side. In the example of Fig. 1, with the substrate grounded, only positive voltages (or ground) are used for NMOS. The source and drain do not conduct significant current to ground, because their junctions are reverse-biased. Therefore if many transistors are constructed on the same substrate they are electrically isolated from each other (unless connected by metal interconnect).

17. The sketch of Fig. 1 is for a transistor off. The same transistor is sketched in Fig.2 for the transistor turned on by applying a large enough positive voltage to the gate (greater than the threshold voltage). The electric field across the relatively thin gate insulator attracts negative charges (electrons) to the surface of the substrate. This effectively provides an N type channel, or electrical connection for negative current flow from the source to the drain, where the word

"drain" is used for the side of the transistor with the larger (more positive) voltage. The transistor is turned off again by removing (or reducing) the gate voltage.

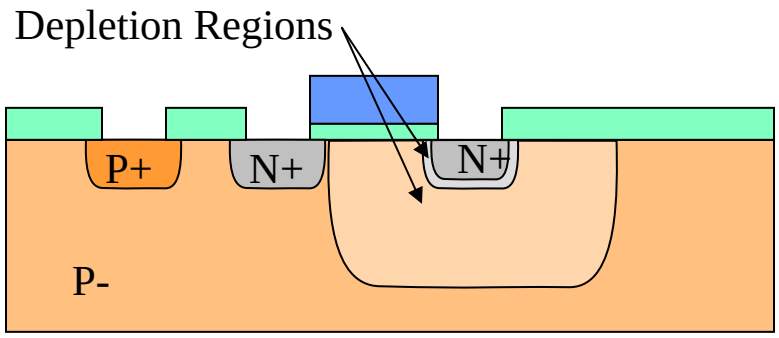
Fig. 2



18. For PMOS transistors, everything is opposite to Fig. 1. P+ type source and drain are constructed within an N- type substrate, and negative voltages are used. Positive current flows from source to drain, with a relatively larger voltage at the drain (more negative).

19. When a reverse-biased voltage is applied to a PN junction, the electric field separates charges, so the regions on both sides of the junction become depleted.

Fig. 3



20. Fig. 3 illustrates the depletion regions for the drain of Fig. 1 (transistor off). The depletion regions are sketched with lighter color tone. The large positive drain voltage attracts N type electrons, depleting the farthest region of the drain, near the junction. The positive drain voltage also repels P type charges (holes), depleting the closest region of the substrate, near the junction. For balanced equal charge, depletion regions are relatively thinner for relatively heavier doping, so the drain depletion is much thinner than the substrate depletion.

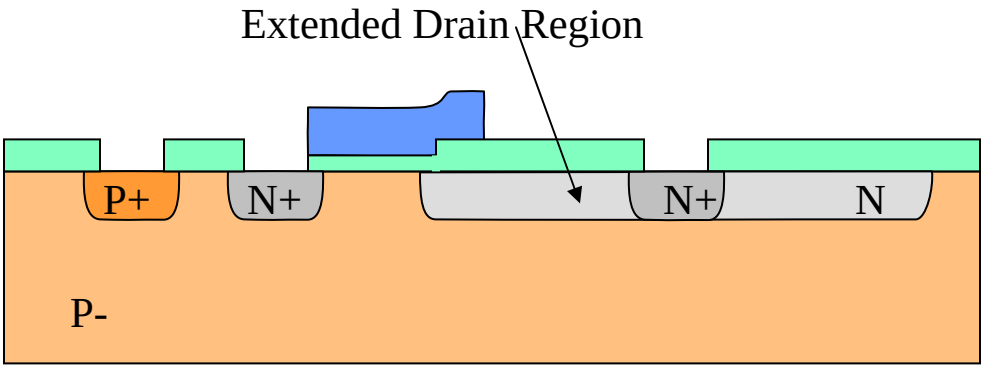
21. The transistor of Fig. 3 can fail when the voltage is large enough for the substrate depletion to "punch through" to the source, causing current to flow, which is one type of high

voltage “breakdown”. This occurs at relatively lower voltages for relatively narrower gates (smaller “gate length” from source to drain). In general, smaller length gates are advantageous for other reasons.

22. Due to this punch through voltage problem (and due to other problems), high voltage transistors can be constructed with a lightly doped drain. A “drain contact” region or “drain contact pocket” still should be heavily doped for electrical contact, but spaced away from the gate, as illustrated in Fig. 4.

23. The transistor of Fig. 4 can therefore be said to have a lightly doped N drain with a heavily doped N+ contact, or it can be said to have an N+ drain with a lightly doped N lateral drift region, as in the introduction to the Beasom ‘173 patent (1:15), or it can be said to have an N+ drain with an offset gate and a lightly doped N extended drain region, as in the introduction to the ‘075 patent (1:19-21). Fig. 4 represents a state of the art high voltage transistor before either patent application.

Fig. 4



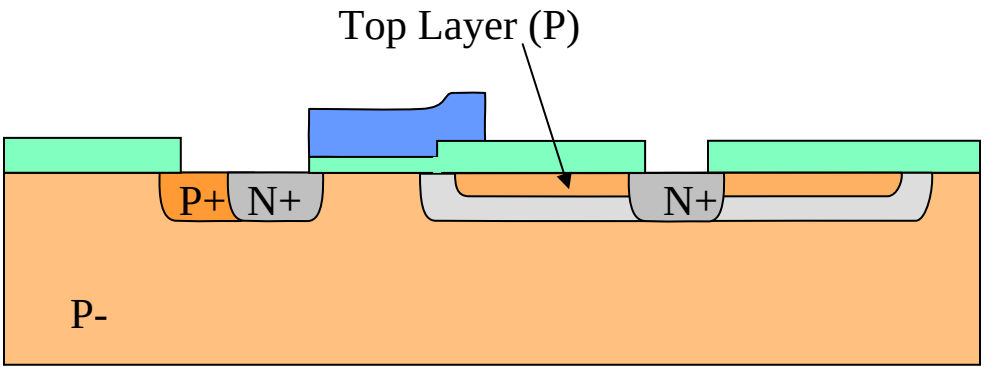
24. The high voltage prior art transistor in Fig. 4 is sketched with the N+ at the same depth as the N, but either can be deeper. The N+ can be wholly within the N, or the N+ can penetrate the N and be partially or mostly within the substrate below, or the N+ can be wholly within the substrate to the right, adjacent to and touching the N region. Fig. 1 of the ‘173 patent illustrates a more complex prior art configuration. These and other configurations produce effective high voltage transistors.

25. The thicker oxide at the gate edge (right in Fig. 4) protects against breakdown from the drain to the gate. The N type extended drain region of Fig. 4 is usually designed to be fully depleted at a drain voltage less than the punch through breakdown voltage, whereby the structure

can withstand a higher drain voltage. A prior art high voltage PMOS transistor is of opposite types.

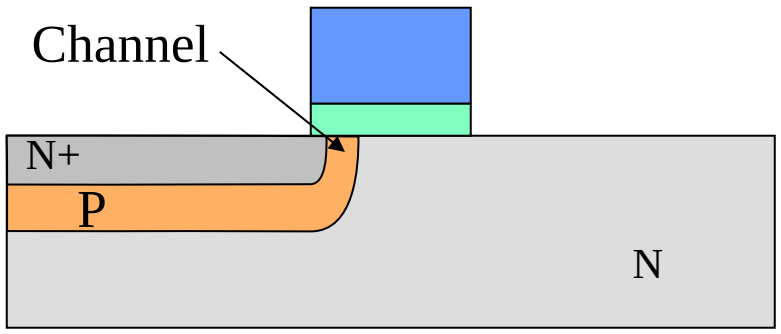
26. The ‘173 patent and ‘075 patent concern improvements whereby a top layer, doped the same type as the substrate, is added to the structure of Fig. 4, as sketched in Fig. 5. The top layer in Fig. 5 is P type. The contacts on the left in Fig. 5 are merged, as is commonly done. Fig. 5 is a sketch of the same transistor structure as illustrated in Fig. 1 of the ‘075 patent. A PMOS version of the same transistor structure is illustrated in Fig. 9 of the ‘173 patent. If called upon, I can provide a more detailed tutorial background concerning the depletion of both the extended drain region and the top layer when high voltage is applied to the drain contact.

Fig. 5



27. **DMOS:** In the structure of figures 1 - 5, the substrate acts as the “base” or “body” or “channel” region. Both the source and the drain are within the substrate in figures 1 - 3, and in figures 4 - 5 the drain contact pocket is within the extended drain, which is within the substrate. In contrast, a DMOS structure has a separate body region. A DMOS source is produced within the body region instead of within the substrate.

Fig. 6



28. Fig. 6 is a minimal sketch of part of one type of DMOS structure. In the example of Fig. 6, the substrate serves as the drain. The effective channel length is defined by the region directly below the gate, and between the N+ source and the N drain, as indicated in Fig. 6.

29. In Fig. 6, the body is more heavily doped than the substrate and the source is more heavily doped than the body. A relatively higher doped channel requires a relatively higher threshold voltage to overcome the opposite doping and to turn on the transistor. Therefore in practice, DMOS structures (with the channel in the relatively higher doped body region) have higher threshold voltages than conventional MOS structures (with the channel in the relatively lower doped substrate).

30. The sketch of Fig. 6 is incomplete. There is usually thick oxide outside the view of the sketch. Heavily doped contact regions, not shown, are usually provided for the body and for the drain.

31. Fig. 6 sketches the substrate as the drain. Other DMOS structures used doped regions within the substrate as the drain. DMOS structures may use drift regions or extended drain regions, and additional doped regions.

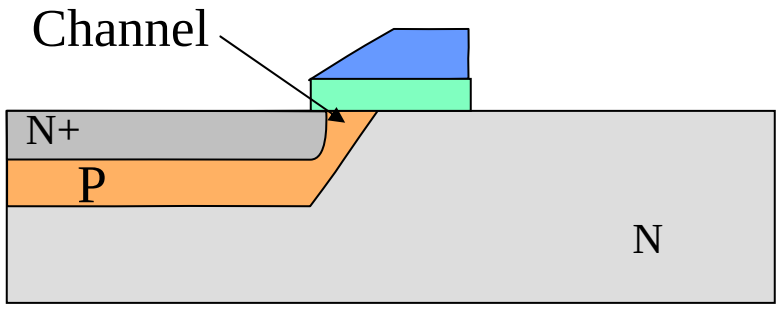
32. The “D” in DMOS means “double diffused” because one process, popular in the past for achieving the structure of Fig. 6, used diffusion doping. Ion implantation has been more popular since the late 1970’s as the preferred method of dopant introduction. Implantation is followed by implant annealing, at which time some diffusion occurs. An implanted DMOS structure is still called a DMOS transistor even if the channel length is defined more by implant lateral scatter distance than by diffusion lateral distance, because the implanted structure is equivalent to the diffused structure.

33. A process for achieving the DMOS structure may be called a “self aligned” process. For example, in Fig. 6, if the left edge of the gate structure serves as the mask for both the base diffusion and the source diffusion, then the channel length is determined by the relative lateral diffusion lengths.

34. Fig. 7 is a sketch of a type of DMOS called DIMOS, where the channel length is primarily determined by the slope of the gate material, and not by diffusion. The contour of the P type body edge of Fig. 7 is determined by the penetration of implanted ions through the variable thickness of the gate material. Although the channel of Fig. 7 is not determined by diffusion, it is considered a type of DMOS because the same channel structure is achieved. Fig.

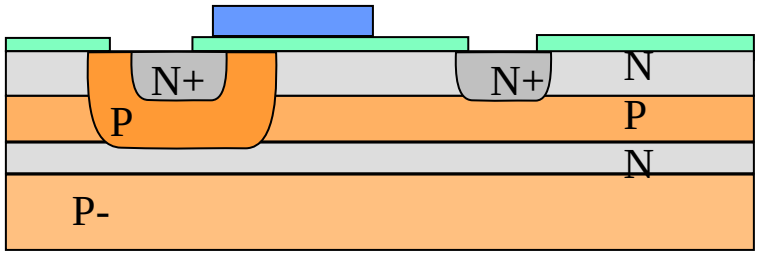
7 is adapted from page 489 of the book by Sze, which is cited as the sole "Other Publications" entry on the face of the '075 patent.

Fig. 7



35. Another example of a DMOS structure is provided by Fig. 1 of the '879 patent by Colak (cited on the face of the '075 patent), sketched as Fig. 8 here, using the same color scheme as the previous figures. Again, the N+ source, on the left, is within the P body region. (The '879 patent indicates n++ for source and p++ for body).

Fig. 8



36. The accused Fairchild structure is simplified and sketched here as Fig. 9, on the last page of this exhibit, next to a copy of Fig. 6 for comparison. The source is within the body region, which is the DMOS structure. Fig. 10 is a less simplified sketch of the accused Fairchild structure, still with the N+ source on the left. The N+ drain is again on the right, with the P top layer sketched on both sides. The P top layer is within the N well, which acts as the extended drain.

37. This exhibit has presented 4 examples of DMOS structure: Fig. 6 simple DMOS, Fig. 7 DIMOS, Fig. 8 Colak DMOS, and Fig. 9 Fairchild DMOS. All 4 structures have the source within a body region and not a source within a substrate. All 4 structures have higher threshold voltage than a structure with a similarly doped substrate serving as the body.

Fig. 9

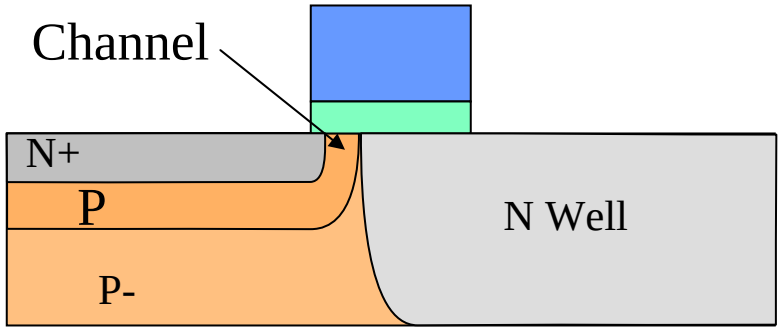


Fig. 6

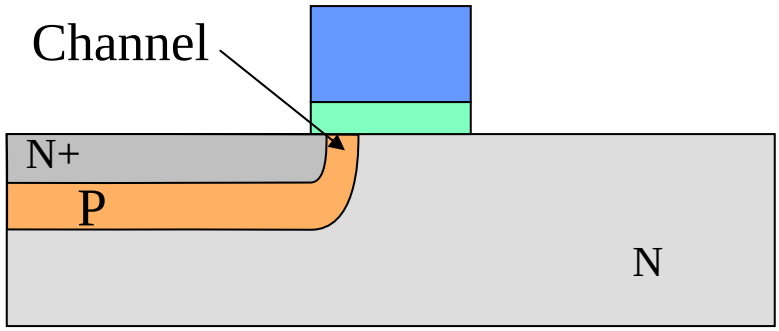


Fig. 10